a source electrode electrically connected to the source layers and the base layer; and

a drain electrode electrically connected to the second main surface of the semiconductor substrate, wherein

93 the semiconductor substrate has an impurity concentration higher than that of the high resistive epitaxial layer and the epitaxial layer intervening between the trenches is depleted in a case where 0 volt is applied between the source electrode and the gate electrodes, and the thickness of a part in the gate insulating films corresponding to the epitaxial layer is thinner than the other parts thereof.

REMARKS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1-30 are pending in the present application. Claims 1, 10 and 14 have been amended by the present amendment.

In the outstanding Office Action, Claims 2, 4, 6, 8, 16, 17, 18, 19, 22, 23, 24, 25, 28 and 29 were indicated as allowable if rewritten in independent form; Claims 1, 9, 10, 14 and 15 were rejected under 35 U.S.C. § 103(a) as unpatentable over Chang et al. in view of Baliga and Korec et al.; and Claims 3, 5, 7, 11, 12, 13, 20, 21, 26, 27 and 30 were rejected under 35 U.S.C. § 103(a) as unpatentable over Chang et al. in view of Baliga, Korec et al. and Singh et al.

Applicants thank the Examiner for the indication of allowable subject matter.

Claims 1, 9, 10, 14 and 15 stand rejected under 35 U.S.C. § 103(a) as unpatentable over Chang et al. in view of Baliga and Korec et al. This rejection is respectfully traversed.

Amended Claim 1 is directed to a power MOSFET including a low resistive semiconductor substrate of a first conductivity type having a first main surface and a second main surface opposing to each other, a drift layer of the first conductivity type formed on the

first main surface of the semiconductor substrate, and a high resistive epitaxial layer of the first conductivity type formed on the drift layer. The power MOSFET also includes trenches formed in the epitaxial layer and the drift layer to extend from a surface of the epitaxial layer into the drift layer, in which the trenches have bottom portions surrounded by the drift layer. Further, the semiconductor substrate has an impurity concentration higher than that of the high resistive epitaxial layer and the epitaxial layer intervening between the trenches is in a state of being depleted in a case where 0 volt is applied between the source electrode and the gate electrodes. Independent Claims 10 and 14 include similar features.

In a non-limiting example, the n-- type base layer 3 shown in FIG. 1 is completely depleted when no voltage is applied between the source electrode 9 and the gate electrodes 6a and 6b (see page 10, lines 5-8). Furthermore, the n- drift layer 2 surrounds the bottom portions of the trenches 4a and 4b. In more detail, the power MOSFET of the present invention does not include P regions at the bottom regions of a pair of trenches 4a and 4b. In other words, the bottom portions of the trenches 4a and 4b are not surrounded by P regions but are surrounded by the n- type drift layer 2 having an impurity concentration higher than that of the base layer 3 as shown in FIG. 1. In an additional non-limiting example shown in FIGS. 4 and 5, the bottom portions of the trenches 4a, 4b and 24a, 24b are surrounded by n+ type substrate 1 and 21 having an impurity concentration higher than that of the base layer 3 and n- type drift layer 22, respectively.

On the contrary, Chang et al. shows in FIG. 1, for example, P regions 122 and 124 formed at the bottom regions of a pair of trenches 104 and 106. When no voltage is applied to the gate connection 134, depletion region 140 is extended from the P regions 122 and 124 to form a potential barrier preventing the flow of current between the drain 130 and source 132 through the mesa region 108 in the N- drift layer 100. In the case of P- drift layer 400

shown in FIG. 5, N regions 222 and 224 are formed to form the depletion region in the similar manner.

Accordingly, it is respectfully submitted independent Claims 1, 10 and 14 and each of the claims depending there from are allowable.

Claims 3, 5, 7, 11, 12, 13, 20, 21, 26, 27 and 30 stand rejected under 35 U.S.C. § 103(a) as unpatentable over Chang et al. in view of Baliga, Korec et al. and Singh et al. This rejection is respectfully traversed.

Claims 3, 5, 7, 11, 12, 13, 20, 21, 26, 27 and 30 depend either directly or indirectly on independent Claims 1, 10 and 14, which as discussed above are believed to be allowable. Further, it is respectfully submitted that Baliga, Korec et al. and Singh et al. also do not teach or suggest the features recited in the independent claims. Therefore, it is respectfully requested this rejection also be withdrawn.

Consequently, in light of the above discussion and in view of the present amendment, the present application is believed to be in condition for allowance and an early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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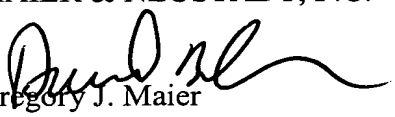

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IN THE CLAIMS

Please amend the claims as follows:

1. (Amended) A power MOSFET, comprising:

a low resistive semiconductor substrate of a first conductivity type having a first main surface and a second main surface opposing to each other;

a drift layer of the first conductivity type formed on the first main surface of the semiconductor substrate;

a high resistive epitaxial layer of the first conductivity type formed on the drift layer;

trenches formed in the epitaxial layer and the drift layer to extend from a surface of the epitaxial layer into the drift layer, the trenches having bottom portions surrounded by the drift layer;

gate electrodes buried in the trenches with gate insulating films interposed between walls of the trenches and the gate electrodes;

low resistive source layers of the first conductivity type formed in a surface region of the epitaxial layer adjacent to the gate insulating films;

a base layer of a second conductivity type formed in the surface region of the epitaxial layer;

a source electrode electrically connected to the source layers and the base layer; and

a drain electrode electrically connected to the second main surface of the semiconductor substrate, wherein

the drift layer has an impurity concentration higher than that of the epitaxial layer and the epitaxial layer intervening between the trenches is depleted in a case where no voltage is applied between the source electrode and the gate electrodes.

10. (Amended) A power MOSFET, comprising:

a low resistive semiconductor substrate of a first conductivity type having a first main surface and a second main surface opposing to each other;

a high resistive epitaxial layer of the first conductivity type formed on the first main surface of the semiconductor substrate;

trenches formed to extend from a surface of the epitaxial layer to the semiconductor substrate, the trenches having bottom portions surrounded by the semiconductor substrate;

gate electrodes buried in the trenches with gate insulating films interposed between the gate electrodes and walls of the trenches;

low resistive source layers of the first conductivity type formed in a surface region of the epitaxial layer adjacent to the gate insulating films;

a base layer of a second conductivity type formed in the surface region of the epitaxial layer;

a source electrode electrically connected to the source layer and the base layer; and

a drain layer electrically connected to the second main surface of the semiconductor substrate, wherein

the semiconductor substrate has an impurity concentration higher than that of the high resistive epitaxial layer and the epitaxial layer intervening between the trenches is in a state of being depleted in a case where 0 volt is applied between the source electrode and the gate electrodes.

14. (Amended) A power MOSFET, comprising:

a low resistive semiconductor substrate of a first conductivity type having a first main surface and a second main surface opposing to each other;

a drift layer of the first conductivity type formed on the first main surface of the semiconductor substrate;

a high resistive epitaxial layer of the first conductivity type formed on the drift layer;

trenches formed to extend from a surface of the epitaxial layer into the semiconductor substrate, the trenches having bottom portions surrounded by the semiconductor substrate;

gate electrodes buried in the trenches with gate insulating films interposed between the gate electrodes and walls of the trenches;

low resistive source layers of the first conductivity type formed in a surface region of the epitaxial layer adjacent to the gate insulating films;

a base layer of a second conductivity type formed in the surface region of the epitaxial layer;

a source electrode electrically connected to the source layers and the base layer; and

a drain electrode electrically connected to the second main surface of the semiconductor substrate, wherein

the semiconductor substrate has an impurity concentration higher than that of the high resistive epitaxial layer and the epitaxial layer intervening between the trenches is depleted in a case where 0 volt is applied between the source electrode and the gate electrodes, and the thickness of a part in the gate insulating films corresponding to the epitaxial layer is thinner than the other parts thereof.